Abstract:

Modern drive control algorithms require advanced hardware &software platforms suitable development process includes in the most cases. The following engineering steps: off-line software simulation, hardware design &software implementation in a target system. This paper presents the general requirements connected with the microprocessor base digital control systems for drive control applications and integrated and flexible hardware and software environment for electric drives control is described. The hardware part of the system includes flexible stand-alone boats and pc cards set basis on the digital signal processor family &advanced field programmable gate arrays (FPGAs). The flexibility of FPGAs provides multiprocessor &open architecture interface. The pc base simulation environment offers hardware-in-the-loops-options &extended data acquisition functions.ofter simulations &evaluations procedures the software structure of the controllers can be transferred into the stand-alone DSP board ready for commercial applications. The proposed integrated systems is very useful in the high performance ac drives &double fed machine controller designs.currently, the project of DSP controller for the voltage source inverter with the power range above 100kw is underway in the Gdansk branch of the Electrotechnical institute several simulation & experimental results are presented & summarized.

## INTRODUCTION:

The technical progress in power electronics, especially in drive control system has been established higher requirements for power devices, signal acquisition and control circuits in the last few years, the most advanced digital technologies were introduced into demanding real time power conversion applications. AICs, DSPs, FPGAs and CPLDs (Complex programmable logic devices), gate arrays.

Modern control algorithms for power conversion equipments require high speed computing, efficient signal capabilities (eg: FET), very fast interrupt response and wide program-data memory spaces. Standard microprocessors or micro controllers do not meet these requirements in many cases such as:

* AC drives with improved dynamic response.
* High performance AC servo drives.
* AC/DC /AC structure with mains and machine inverter.
* Double fed machine control systems.
* Fast mains compensators (active filters).
* Advanced UPS.

In mentioned applications the control system processor must perform a lot of computing-intensive and time critical tasks; PWM procedure software controllers algorithms estimation and transformation of state variables, software models and observers, protection and auto diagnostics function, external communications protocol.

Quite a few integrated micro controller (SAB8OC166/167family){1} or microprocessors (1960 embedded /super scalar processor family)[2] can only provide satisfactory performance. Several experimental applications based on transputer technology and ASICs have been presented in subject literature. However, the combination of DSP features (high performance, high power and cost effectiveness) makes this technology the most significant in R&D and commercial applications. The processor kernel of the digital control system usually requires a glue logic system and various I/O subsystems with special functions like:

* Dedicated I/O set for analog signal acquisition and generation (ADCs/DACs).
* Interfaces for absolute and incremental encoders and other frequency signals.
* General purpose digital I/O.
* Digital communication interfaces for a wide range of industrial standards (RS-232, RS-422, RS-485, current loop, fibre optic).
* MMIs (man machine interfaces).

It is practically impossible to implement the complex digital functions by means standard VLSI integrated and/or traditional PAL/GAL devices. These ASIC and gate arrays technologies are relatively expensive. The NRE (Non recurring engg.)Costs are significant because the engineering process tended to take months to complete silicon and chip prototype design cycle. The optimal alternative for flexible and integrated implementations of the medium and complex logical structure are field programmable logic arrays (FPGAs) and EPROM or flash based complex programmable logic devices (CPLDs).

Achieving research or commercial goal requires specialized software and flexible hardware tools. The integrated solutions must provide high efficiency during a research and experimental period with fast migration capabilities into the commercial target system.

## 2:A SUMMERY OF THE ART STATE IN “DSP” AND “FDGA” TECHNOLOGY:

The beginning of the 90s has established the rapid progress in the DSP technology. Over the past 5 years, many important parameters have been improved. The cycle time has dramatically decreased from approximately 20nsec to15nsec. The internal RAM capacity has increased over 50Kbytes the leading DSP manufacturers have been preparing a broad range of universal families and dedicated model for specialized tasks and high volumes applications (telecommunications, voice processing, multimedia). The communication capabilities have been continuously extended by addition of synchronous and asynchronous serial ports, multiprocessor links and DMA channels. The additional advanced features are implemented in the modern DSPs: power management options software programmable wait-state generator, the JTAG interface efficient debugging in target system and various signal-processing enhancements. The customized versions of digital signal processors are available (CDSP).

Fixed point DSP families provide processing range unto 66 MIPS. The new floating-point devices bring a new power of DSP processing into cost-sensitive applications. The floating-point units have more efficient architecture for high-level language (HLL) compilers.

The software solutions for DSPs consists of: basic software tools (assembler, linkers), HLL debugger and application development environments (MATLAB, PTHOLEMY), the high-speed computing architecture of DSP is attractive for fuzzy-logic processing and offers the performance similar to hardwired fuzzy-logic processors. The world’s leading DSP suppliers begin to offer fully integrated windows-based tools for fast code development and debugging.

Experimental digital control systems with digital signal processors have been presented in many technical publications on drives control technology and power conversion. Some modern commercial power electronic products are equipped with DSPs3.

The first programmable logic devices (LD) were shipped in the beginning of 80s.the small PAL/GAL structure has many disadvantages: small logical resources high, power consumption, one-time programming cycle (PALs) are external reprogramming in specialized programmers (GALs). The number of programming cycles and debugging capabilities were limited. The development tools have been supporting only simple options.

The world’s first EPGAs were introduced in 1985. However their costs were too high to provide economical efficiency in the wide range of digital designs until the end of 90s. Recently introduced families offer over 100K logical gates capacity. The number of benchmark speeds achieves above 100MHz.some internal logical structures can be performed with the operating frequency up to 150MHz.

Modern FPGA devices are equipped with power saving modes and debugging interface in JTAG standard. JTAG allows multiple and various devices to be daisy-chained. This simplifies PCB layout, minimizes hardware overhead and reduces test software requirements.

FPGA development process is supported by specialized software tools. Typical

Design flow includes the following steps:

* Design entry: schematic, HDL (hardware description language), waveforms, Boolean with mixed structure options.
* Compilation and logic optimization
* Mapping, place and route
* Interactive simulation and timing analysis
* Optional-floor-planning
* Design verification and in circuit hardware debugging.

The most advanced development software tools support a wide range of library modules. Sophisticated libraries of DSP macro functions are currently available. Windows based software environment is a standard.

However, as time to market pressure increases, designers are constantly demanding more efficiency and power from programmable logic devices and software tools during designing process of both simple and complex logical structures. The leading manufacturers of FPGA solutions constantly improved their features.

FPGA technology enhancements can be summarized in the following points:

* High logical capacity devices minimize part and connection count on PCBs.
* Power consumption is significantly reduced
* Noise immunity and reliability of control system is increasing
* Field diagnostic and customer upgrade is available
* One hardware module can be configured for different applications
* NRE costs are limited
* Advanced development software tools provide flexible design entry, simulation and verification a target system.

All mentioned features are very profitable in power electronic designs.infact, the heart of modern digital Control system includes both DSP and FPGA technology.

**3.INTEGRATED CONTROLLER ARCHITECTURE**

During the development process of digital control system many conceptions and technical problems must be overcome to achieve Optimum results. The integrated system idea presented in this paper has been developed in the Gdansk Branch of the Electrotechnical Institute. It is a choice among many conceptions that have been made based-on technical and economical analysis.

The strategy of an integrated controller defines two compliments parts: hardware and software development solutions. The hardware part includes stand-alone boards and PC cards set based-on DSPs and FPGAs the software environment consists of PC-based simulation software package tailored for the drive technology purposes, communication procedures, DSP code generation tools and FPGA

Development solutions.

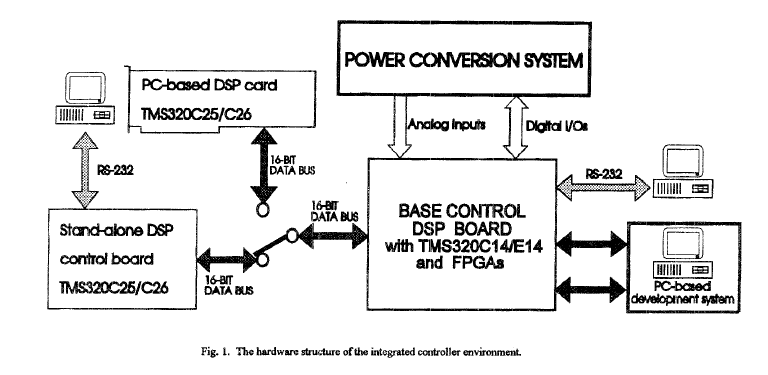


Fig: 1 presents an overview of the hardware structure: the sample configuration of the flexible system useful for high performance electric drives

Control algorithm protyping and evaluation. The base control DSP board with the TNS320C14/E14 processor and FPGA devices. Provides the direct interface between a physical layer of the frequency converter and external coprocessor subsystems.

The universal coprocessor PC card based on the TMS320C25/C26 fixed point DSP family is used during the Simulation and experimental period. During laboratory tests of the drive the PC card is connected with the baseboard via fast parallel interface (16-bit). The commercial target version of the control system can be easily achieved by using the stand-alone DSP board. it has the similar internal structure as the PC card, but without PC-host interface. A DSP code performed on PC card needs only small corrections to relocate into stand-alone DSP board.

The stand-alone DSP board enables several codes

* Direct execution from fast EPRQM/E2PRQM/FLASH,
* Reloading from slower ROM-type memory into

Executable RAM.

* Code loading via universal RS-232 interface into

Executable RAM (user loading program resides in ROM-type memory.),

* External code boot-loading option (TMS320C26 only).

The above-mentioned stand-alone board is mechanically compatible with base control D**SP** board. It makes possible the connection the another model ***of*** the co-processor

Board with a different **type** of a micro controller or DSP (e.g. floating-point unit based-on the TMS320C31). The flexibility of FPGAs provides multiprocessor and open

Architecture interfaces.

The internal structure of the base control board is shown in Fig. 2. The TMS32OC14E14 is the first generations family member dedicated to embedded control applications (instruction cycle max. 160ns). It is, equipped with extended RW/timing capabilities watchdog, asynchronous& synchronous serial port, bit selectable I/OS and compare capture subsystems. Three FPGA devices define: the separate and flexible interface logic for inputs, outputs and communication purposes the logic's definitions are stored in the configuration PROMS. Advanced so software tools enable fast changes in FPGA structures during thedevelopment process. It is possible to prepare several logical structures of the base control board and improve timing performanceby using the higher capacity and faster devices.

The software part of the integrated solution consists of two similar modules:

* The FAL module, dedicated for co-operation with PC based

Dsp cards via internal PC bus.

* The FaGRS module, which uses serial interface.

Both software modules FAL and FAL-RE; are originally developed in the Gdansk branch of the Electro technical Institute. The simulation software offers hardwire-in-the-loop option and extended data acquisition functions. The DSP programs can be compiled and loaded into PC card or stand alone board in parallel or serial mode, respectively. All functions are available in the single integrated environment.

During the simulations the motor-load subsystem can be implemented as a program in The PC: The digital controller code resides on the DSP PC-based card and it

Can be easily reloaded. Both programs are communicated with each other. Since simulation and evaluation procedures have been done, the software structure of the

DSP controller could be transferred into the stand-alone DSP board ready for commercial use.

The FAL module has built-in oscilloscope-like options for real-time variables monitoring and waveforms displaying thanks, to continuous bi-directional communication with the DSPcontroller application on PCcard. The waveforms of up to8 variables can be simultaneously presented: motor or mainsphase currents and voltages,



Dc voltage, Dc current, rotor flux and other estimated internal variables of an induction machine, vector numbers sequence. Acquired data can be saved on disk in the ASCI format.

The limited data acquisition capabilities are provided in the FAL-RS module Real-time data monitoring is disabled. The limited-time window of data can be stored in the internal RAM of the stand-alone DSP card after defined triggering conditions. Then acquired data samples are serially transmitted and continuously refreshed. Selected numerical and variable can be defined and observed continuously with out graphical representation.

The typical software development procedure in the presented integrated environment includes:

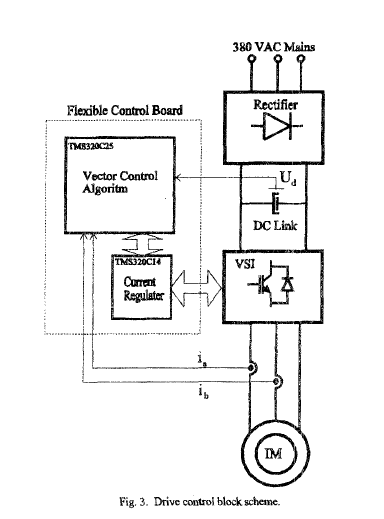
* PC-BASED SIMULATION-both software sections the digital controller and the motor load subsystem are implemented in the high-level language(C/C++) or MATLAB on the PC platform.
* HARDWARE-IN-THE –LOOP SIMULATION-digital controllers code resides on PC based DSP cards, the motor-load subsystem is defined as the program in the high-level language(C/C++) on the PC platform.
* LABORATORY EXPERIMENTS- the PC based DSP card resides in PC-host environment and is connected with the base control DSP board, experiments with real power converter –motor-load structure are performed, while the previous simulation steps are continuously available.
* STAND ALONE OPERATIONS TESTS – the target version of the DSP controller software is evaluated; limited data acquisition and monitoring capabilities are enabled.

The above mentioned scheme has been explored during the control algorithms of the high – performance drive development in the Gdansk branch of the Electrotechnical institutes .the results of properly defined simulations are similar to practical implementations.

EXAMPLE OF EXPERIMENTAL APPLICATIONS

### A: control structure

The flexible control boards have been used in a vector control induction motor drive system, presented in fig.3.



The induction motor is fed by the current controlled voltage source inverter (VSI). The speed sensorless vector controller [4] [5] [6] estimates rotor flux vector and speed using stator currents and voltages are not measured from the motor terminals, but are evaluated from the measured dc link voltage Ud, and pulse trains generated by the current controller. The estimated rotor speed is used as feedback in speed control loop. The estimated rotor flux is used to decompose the stator current vector to the torque and flux-producing component. The flux producing component (magnetizing current is used in the flux magnitude control loop. The PI controllers are used in both loops.

**B: simulation results**

The performance of the presented controller was first tested by simulation. An 110KW induction motor is represented by its dynamic equations as a software model in a PC computer. The control structure structure and the current regulator are implemented in assembler language on the TMS320C25 digital signal processor board working in PC computer environment. During simulations the timing requirements of the controller procedures were confirmed and the PI controllers parameters have been tuned.

The transient state of the simulations is shown in fig.4 and 5. The motor is started with a speed reference value equal to the rated value

 A quadratic load torque/speed characteristic is assumed. The measured speed  and estimated speed  are presented on fig.4 and 5 shows stator current component is a and rotor flux magnitude during the same transient state. Before the motor starting, the controller generates a dc current into stator to excite the machine (rotor flux magnitude reaches its normal value). This procedure for t<0 is not shown in the fig.5





The drive dynamic behavior is defined by the stator current regulator limits and the flux magnitude regulator.



TABLE 1 represents processing times of some functions implemented on the TMS320c25 DSP (with 100nsec instruction time). All the data are 16 bit words.

## C: experimental results

In the experimental released of the drive system, the control tasks are divided into two DSP processor. The current regulator has been implemented on the TMS320C14 signal processor on the base control DSP board. The vector control algorithm has been implemented on the TMS320C25 signal processor on the stand-alone DSP board. This processor performs the flux and speed estimation, the control loops and manages the A/D conversions. A sampling period of the control algorithms is equal to 400 microseconds. The computing time is much shorter, about half of the sampling period. Remaining time is used for monitoring and communication functions. The stator currents measured and referenced values are transferred from TMS320C25 to TMS320C14 processor through two 16-bit buffers. Interrupts from A/D converter synchronize the analog measurements and current regulator.



The motor used in experiments in a 5KW squirrel cage induction machine. Fig: 6 show an example behavior of the motor with exponential reference speed from 0 to 0.5 rated value. The reference and estimated rotor speed and a component of stator current are shown on the same fig. Although machine is working with no load there are no speed oscillations in the study state.

Thanks to TMS320C14 with built-in watchdog timer and feedback error signals from the VSI, the current regulator guaranties high level of protection and reliability. Estimation of speed measurements and reliability and minimization of other analogue values measurement made further improvements of the reliability of the drive system.

CONCLUSION:

The flexible and integrated development system consists of the hardware and the software part. The technology, the software consists of two similar modules. FAL and FAL-RS. Both system parts have been built in the Gdansk branch of Electrotechnical Institute. The presented system makes possible PC simulations and real-time implementation of sophisticated sensorless drive control algorithms. The experimental results approve the high usefulness and advantages of DSP and FPGA solutions for advanced drive control purposes. The proposed sensorless drive control algorithm includes the original features such as high accuracy and fast response time. The target laboratory experiments have been started with 110KW VSI semi-commercial model. Currently the real-time dynamic performance of the mentioned algorithms is evaluated with the 110KW drive system.

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